

**CSE 231 Term Project**

**Spring-2018**

**Section: 02**

**Phase 1: Combinational Circuit Design**

**Submitted By: Group: 01**

**Group Members:**

|  |  |
| --- | --- |
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**Submission date: 16/04/18**

**Submitted to:**

**Professor Dr. Arshad M Chowdhury**

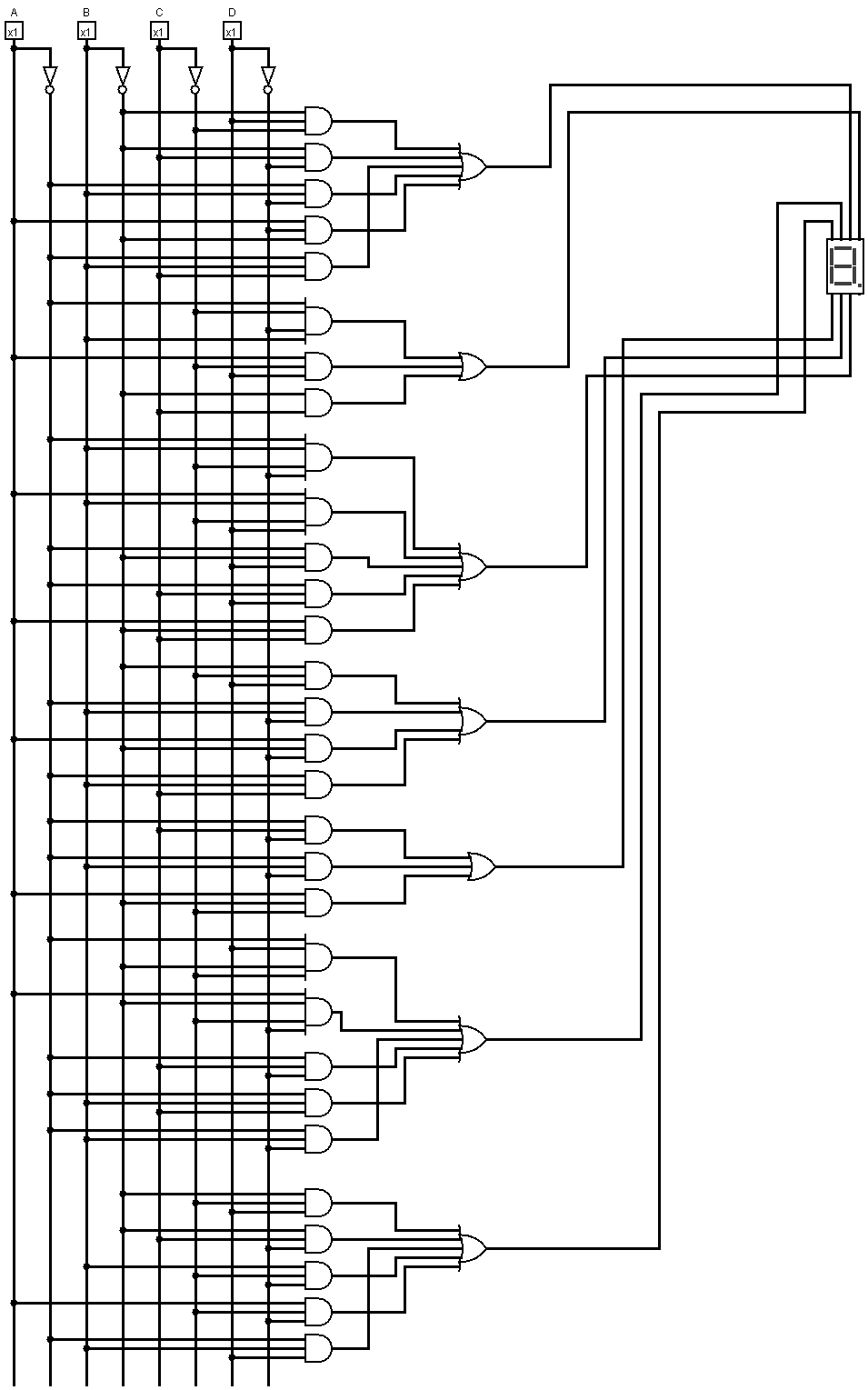
**Phase 1: Combinational Circuit Design**

**Objectives**:

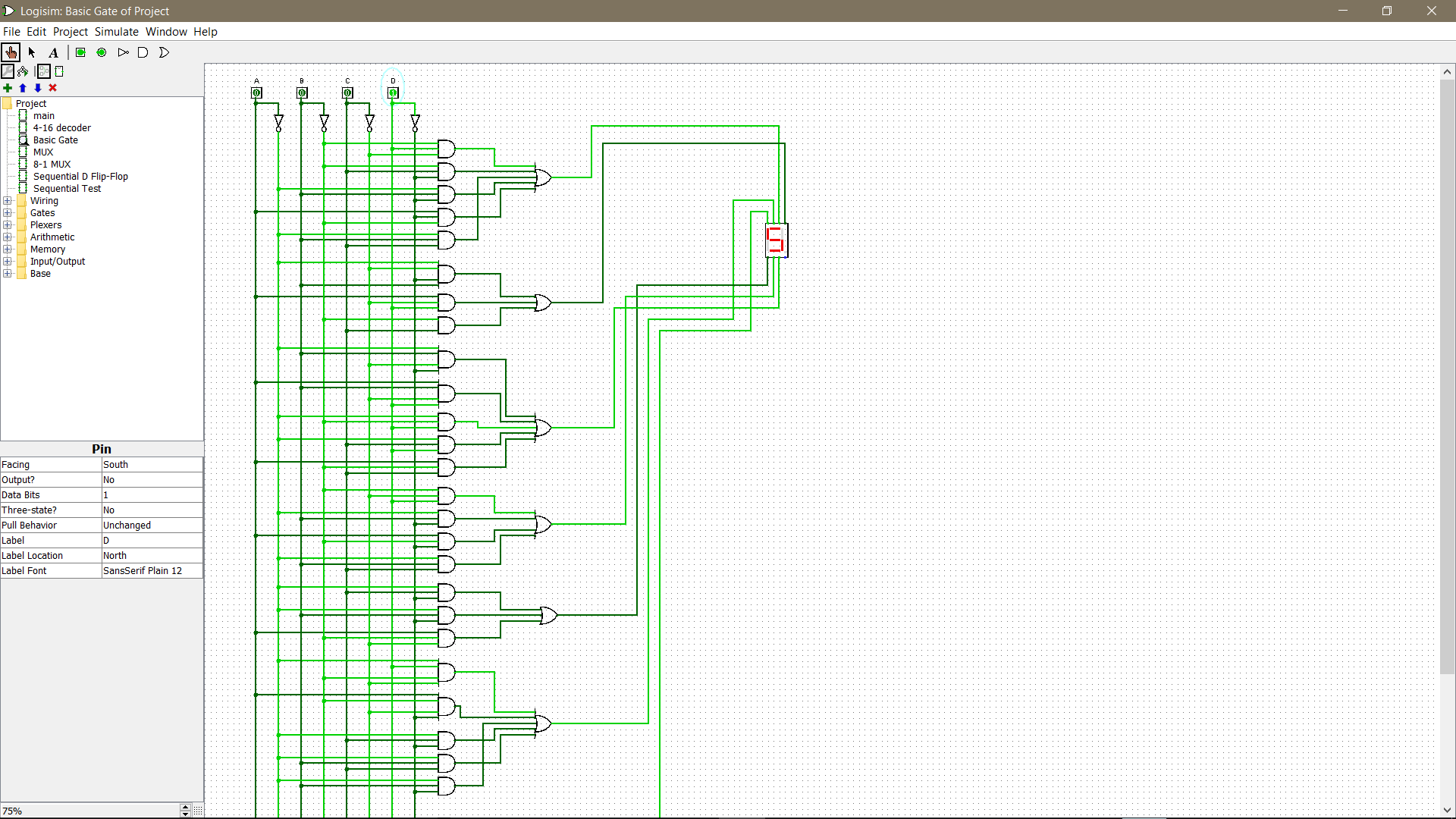
* Design the combinational logic part of the system to display the characters of the string on a seven-segment display
* Simulate the circuit with Logisim.

**Using universal / basic gates with Minimal logic implementation**

1. **Circuit Diagram:**



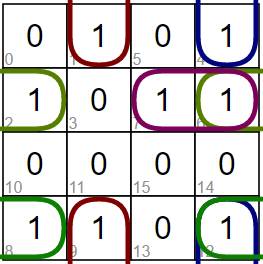
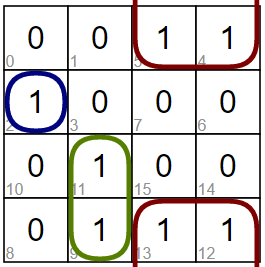
1. **Simulation:**



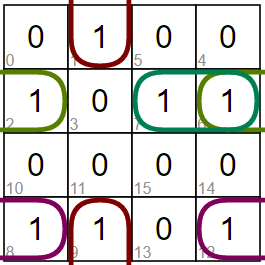
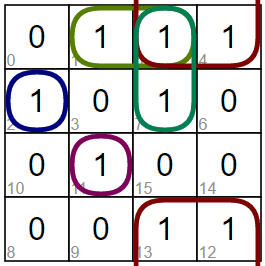
1. **Truth Table:**

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **D** | **F** | **a** | **b** | **c** | **d** | **e** | **f** | **g** |
| **0** | **0** | **0** | **0** |  | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **0** | **0** | **0** | **1** | **S** | **1** | **0** | **1** | **1** | **0** | **1** | **1** |
| **0** | **0** | **1** | **0** | **P** | **1** | **1** | **0** | **0** | **1** | **1** | **1** |
| **0** | **0** | **1** | **1** | **1** | **0** | **1** | **1** | **0** | **0** | **0** | **0** |
| **0** | **1** | **0** | **0** | **8** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **0** | **1** | **0** | **1** | **-** | **0** | **0** | **0** | **0** | **0** | **0** | **1** |
| **0** | **1** | **1** | **0** | **C** | **1** | **0** | **0** | **1** | **1** | **1** | **0** |
| **0** | **1** | **1** | **1** | **S** | **1** | **0** | **1** | **1** | **0** | **1** | **1** |
| **1** | **0** | **0** | **0** | **E** | **1** | **0** | **0** | **1** | **1** | **1** | **1** |
| **1** | **0** | **0** | **1** | **2** | **1** | **1** | **0** | **1** | **1** | **0** | **1** |
| **1** | **0** | **1** | **0** | **3** | **1** | **1** | **1** | **1** | **0** | **0** | **1** |
| **1** | **0** | **1** | **1** | **1** | **0** | **1** | **1** | **0** | **0** | **0** | **0** |
| **1** | **1** | **0** | **0** | **-** | **0** | **0** | **0** | **0** | **0** | **0** | **1** |
| **1** | **1** | **0** | **1** | **1** | **0** | **1** | **1** | **0** | **0** | **0** | **0** |
| **1** | **1** | **1** | **0** |  | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **1** | **1** | **1** | **1** |  | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

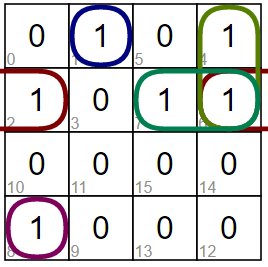
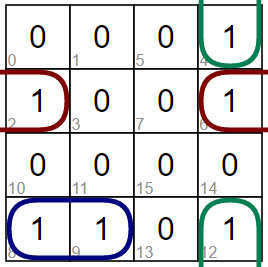
1. **K-Maps:**



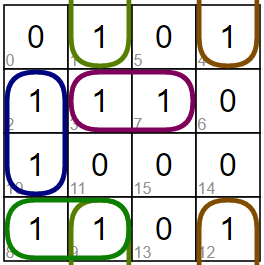
**a = B’C’D + B’CD’ + A’BD’ + AB’D’ + ABC b = A’BC’D’ + AC’D + B’C**



**c = A’BC’D’ + ABC’D + A’B’D + A’CD d = B’C’D + B’CD’ + A’BD’ + AB’D’+ A’BC**



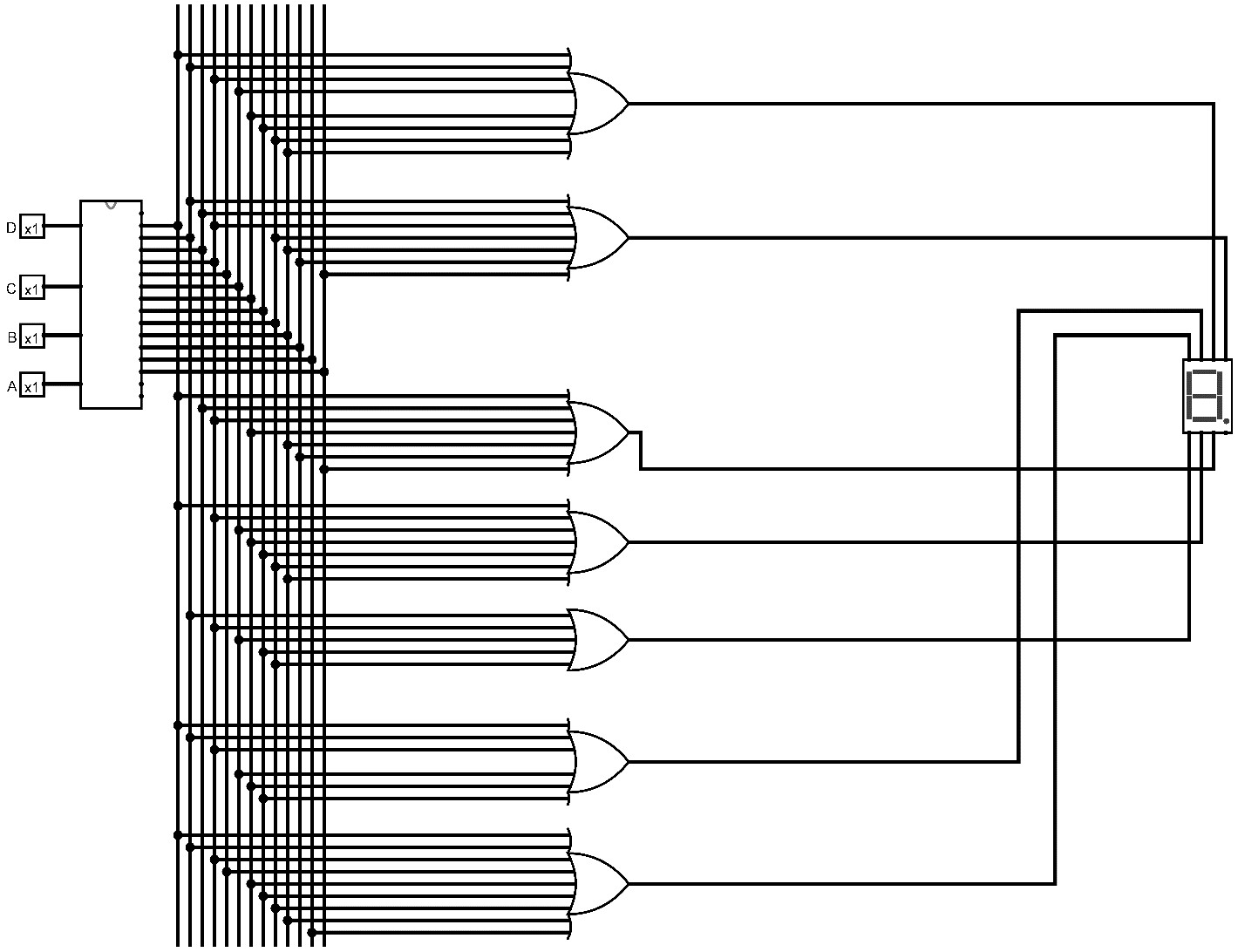
**e = A’CD’ + A’BD’ + AB’C’ f = A’B’C’D + AB’C’D’ + A’CD’ + A’BD’ + A’BC**



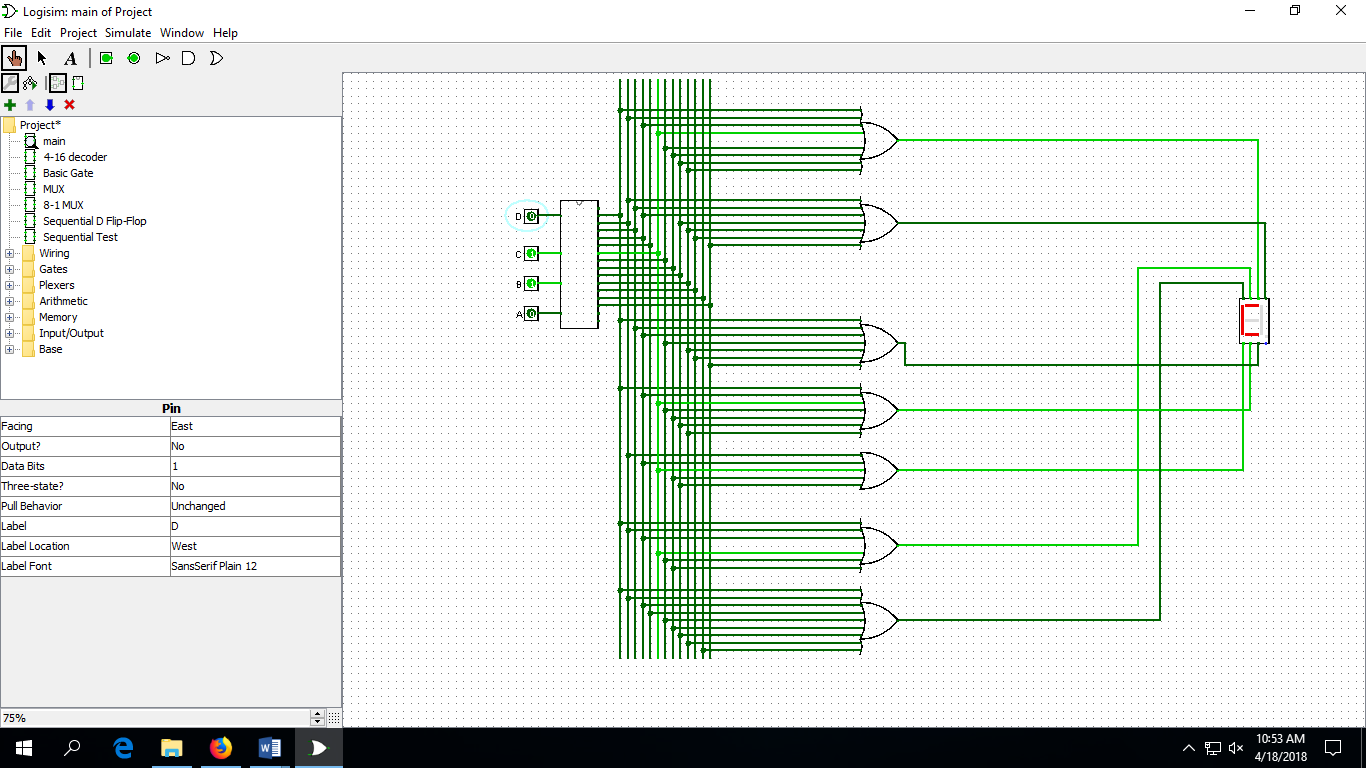
**g = B’C’D + B’CD’ + BC’D’ + AC’D’ + A’BD**

**Using Decoder (3:8)**

1. **Circuit Diagram:**

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1. **Simulation:**



1. **Truth Table:**

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **D** | **F** | **a** | **b** | **c** | **d** | **e** | **f** | **g** |
| **0** | **0** | **0** | **0** |  | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **0** | **0** | **0** | **1** | **S** | **1** | **0** | **1** | **1** | **0** | **1** | **1** |
| **0** | **0** | **1** | **0** | **P** | **1** | **1** | **0** | **0** | **1** | **1** | **1** |
| **0** | **0** | **1** | **1** | **1** | **0** | **1** | **1** | **0** | **0** | **0** | **0** |
| **0** | **1** | **0** | **0** | **8** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **0** | **1** | **0** | **1** | **-** | **0** | **0** | **0** | **0** | **0** | **0** | **1** |
| **0** | **1** | **1** | **0** | **C** | **1** | **0** | **0** | **1** | **1** | **1** | **0** |
| **0** | **1** | **1** | **1** | **S** | **1** | **0** | **1** | **1** | **0** | **1** | **1** |
| **1** | **0** | **0** | **0** | **E** | **1** | **0** | **0** | **1** | **1** | **1** | **1** |
| **1** | **0** | **0** | **1** | **2** | **1** | **1** | **0** | **1** | **1** | **0** | **1** |
| **1** | **0** | **1** | **0** | **3** | **1** | **1** | **1** | **1** | **0** | **0** | **1** |
| **1** | **0** | **1** | **1** | **1** | **0** | **1** | **1** | **0** | **0** | **0** | **0** |
| **1** | **1** | **0** | **0** | **-** | **0** | **0** | **0** | **0** | **0** | **0** | **1** |
| **1** | **1** | **0** | **1** | **1** | **0** | **1** | **1** | **0** | **0** | **0** | **0** |
| **1** | **1** | **1** | **0** |  | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **1** | **1** | **1** | **1** |  | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

1. **Functions:**

**a = m1 + m2 + m4 + m5 + m6 + m7 + m8 + m9**

**b = m2 + m3 + m4 + m9 + m10 + m11 + m13**

**c = m1 + m3 + m4 + m7 + m10 + m11 + m13**

**d = m1 + m4 + m6 + m7 + m8 + m9 + m10**

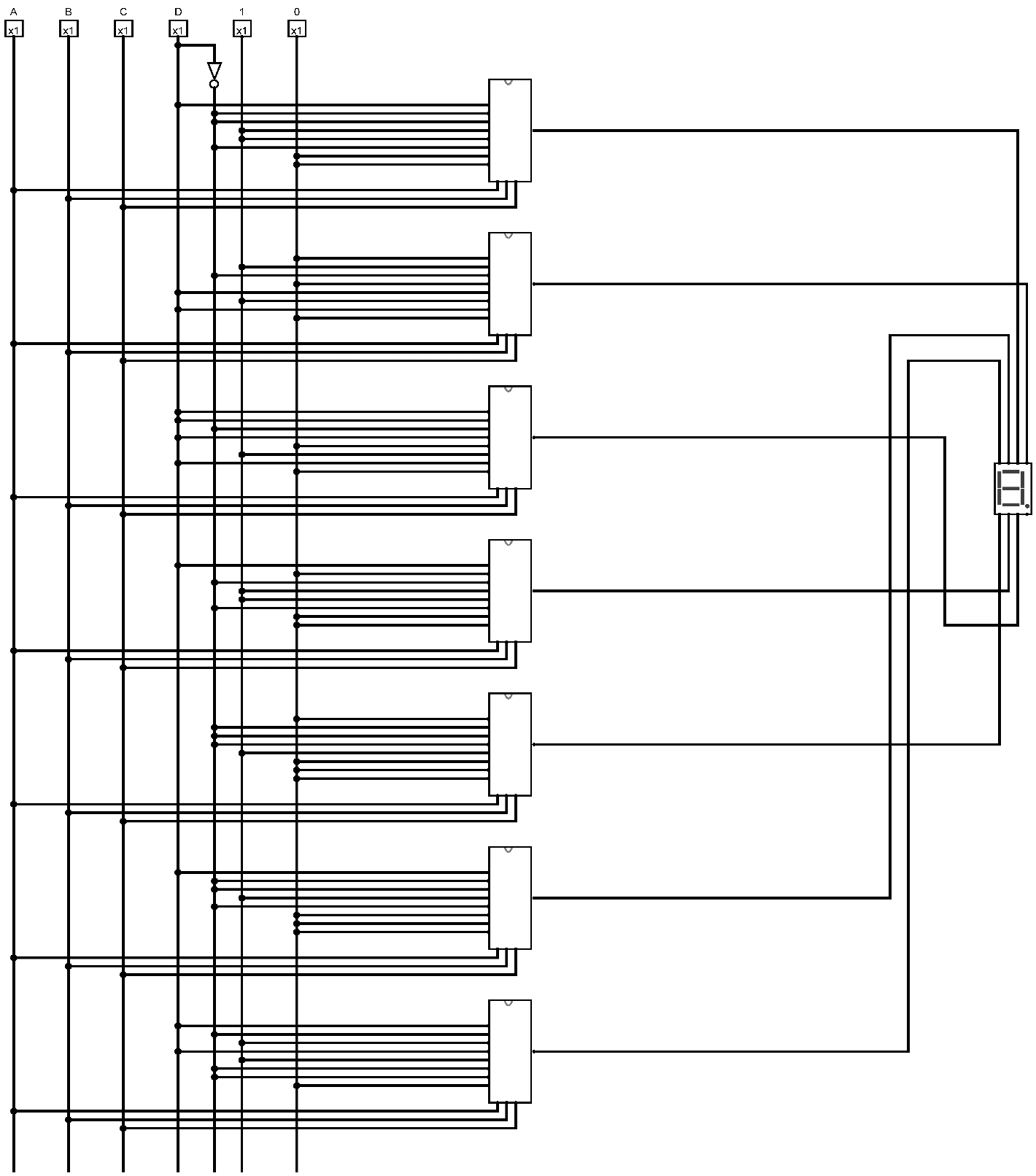
**e = m2 + m4 + m6 + m8 + m9**

**f = m1 + m2 + m4 + m6 + m7 + m8**

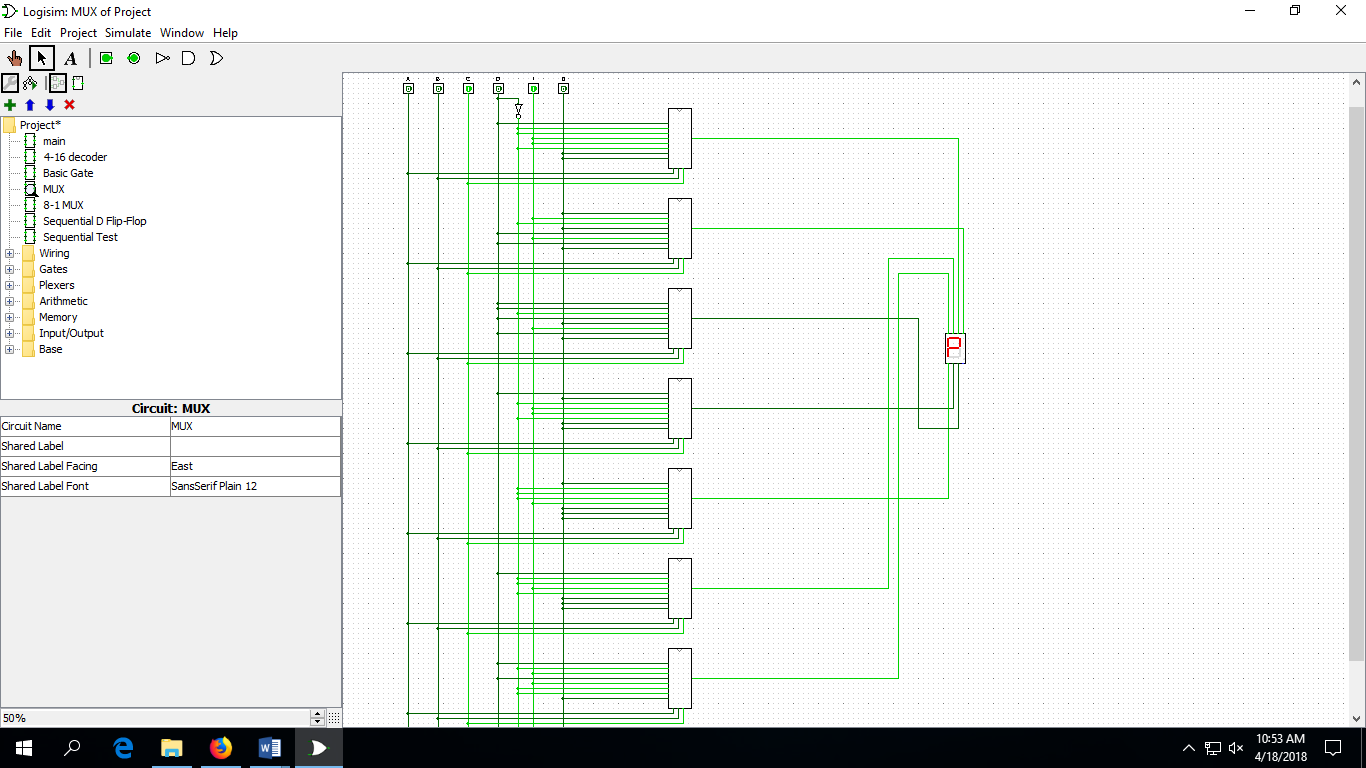
**g = m1 + m2 + m4 + m5 + m7 + m8 + m9 + m10 + m12**

**Using 8 to 1 Line Multiplexer**

1. **Circuit Diagram:**

****

1. **Simulation:**



1. **Truth Table:**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **D** | **F** | **a** |  | **b** |  | **c** |  | **d** |  | **e** |  | **f** |  | **g** |  |
| **0** | **0** | **0** | **0** |  | **0** | **I0=D** | **0** | **I0=0** | **0** | **I0=D** | **0** | **I0=D** | **0** | **I0=0** | **0** | **I0=D** | **0** | **I0=D** |
| **0** | **0** | **0** | **1** | **S** | **1** | **0** | **1** | **1** | **0** | **1** | **1** |
| **0** | **0** | **1** | **0** | **P** | **1** | **I1=D’** | **1** | **I1=1** | **0** | **I1=D** | **0** | **I1=0** | **1** | **I1=D’** | **1** | **I1=D’** | **1** | **I1=D’** |
| **0** | **0** | **1** | **1** | **1** | **0** | **1** | **1** | **0** | **0** | **0** | **0** |
| **0** | **1** | **0** | **0** | **8** | **1** | **I2=D’** | **1** | **I2=D’** | **1** | **I2=D’** | **1** | **I2=D’** | **1** | **I2=D’** | **1** | **I2=D’** | **1** | **I2=1** |
| **0** | **1** | **0** | **1** | **-** | **0** | **0** | **0** | **0** | **0** | **0** | **1** |
| **0** | **1** | **1** | **0** | **C** | **1** | **I3=1** | **0** | **I3=0** | **0** | **I3=D** | **1** | **I3=1** | **1** | **I3=D’** | **1** | **I3=1** | **0** | **I3=D** |
| **0** | **1** | **1** | **1** | **S** | **1** | **0** | **1** | **1** | **0** | **1** | **1** |
| **1** | **0** | **0** | **0** | **E** | **1** | **I4=1** | **0** | **I4=D** | **0** | **I4=0** | **1** | **I4=1** | **1** | **I4=1** | **1** | **I4=D’** | **1** | **I4=1** |
| **1** | **0** | **0** | **1** | **2** | **1** | **1** | **0** | **1** | **1** | **0** | **1** |
| **1** | **0** | **1** | **0** | **3** | **1** | **I5=D’** | **1** | **I5=1** | **1** | **I5=1** | **1** | **I5=D’** | **0** | **I5=0** | **0** | **I5=0** | **1** | **I5=D’** |
| **1** | **0** | **1** | **1** | **1** | **0** | **1** | **1** | **0** | **0** | **0** | **0** |
| **1** | **1** | **0** | **0** | **-** | **0** | **I6=0** | **0** | **I6=D** | **0** | **I6=D** | **0** | **I6=0** | **0** | **I6=0** | **0** | **I6=0** | **1** | **I6=D’** |
| **1** | **1** | **0** | **1** | **1** | **0** | **1** | **1** | **0** | **0** | **0** | **0** |
| **1** | **1** | **1** | **0** |  | **0** | **I7=0** | **0** | **I7=0** | **0** | **I7=0** | **0** | **I7=0** | **0** | **I7=0** | **0** | **I7=0** | **0** | **I7=0** |
| **1** | **1** | **1** | **1** |  | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

**Explanation**

In our Project, we were instructed to print “SP18-CSE231-1” in a single 7 segment decoder display. There are 13 letters in this sentence so we need to use at least 16 combinations. And for 16 combinations we need 4 variablse. Our four variable is A, B, C, D. From the truth table it can be seen that, the number of input bits is four (A, B, C, D) and the number of output bits is seven (a,b,c,d,e,f,g). In our circuit we started to print the sentence form 0001 combination. So that’s why we assigned all the 13 letters from 0001 to 1101 respectively. For the combination 0000, 1110 and 1111, we considered that there will be no output in 7 segment display.

Afterwards,we have constructed the truth table accordingly and with the help of the K-map we obtained minimal term for each of the seven output functions (a,b,c,d,e,f,g). Later,we have simulated the circuit with logisim with basic gates, 3:8 decoder and 8:1 multiplexar.

However, we have chosen to conduct the experiment using multiplexar.Behind this decision we had to consider a few facts like number of bits, efficiency, complexity, cost consideration etc. We found that if we use 8:1 multiplexer then there will be least amount of IC’s where only 7 piece of 74151 IC and only one 7404 IC. Apart from this, we needed a less amount of wires which gives less amount of complexity.

From the above given figure it can be seen that for both basic gates and decoder the Literal cost (L), Gate input cost (G), Gate input cost including inverters (GN) are much higher than the multiplexar.Also it will be a very complicated circuit where relatively more wiring is required and also the cost of implementation is higher.Thus we have decided to use multiplexar to implement the circuit.